

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40244B

buffers

Octal buffers with 3-state outputs

Product specification
File under Integrated Circuits, IC04

January 1995

Octal buffers with 3-state outputs

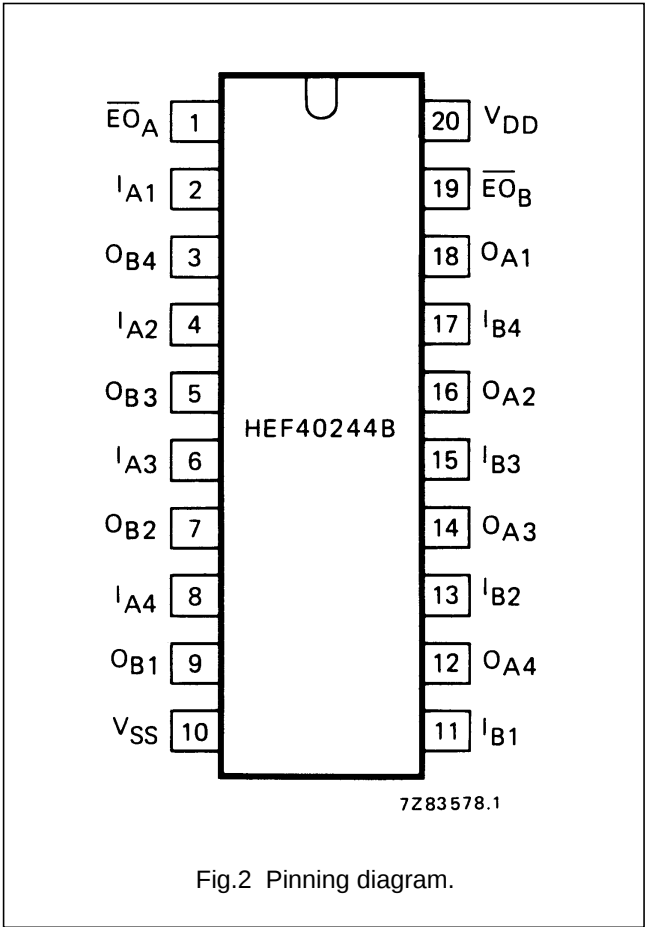
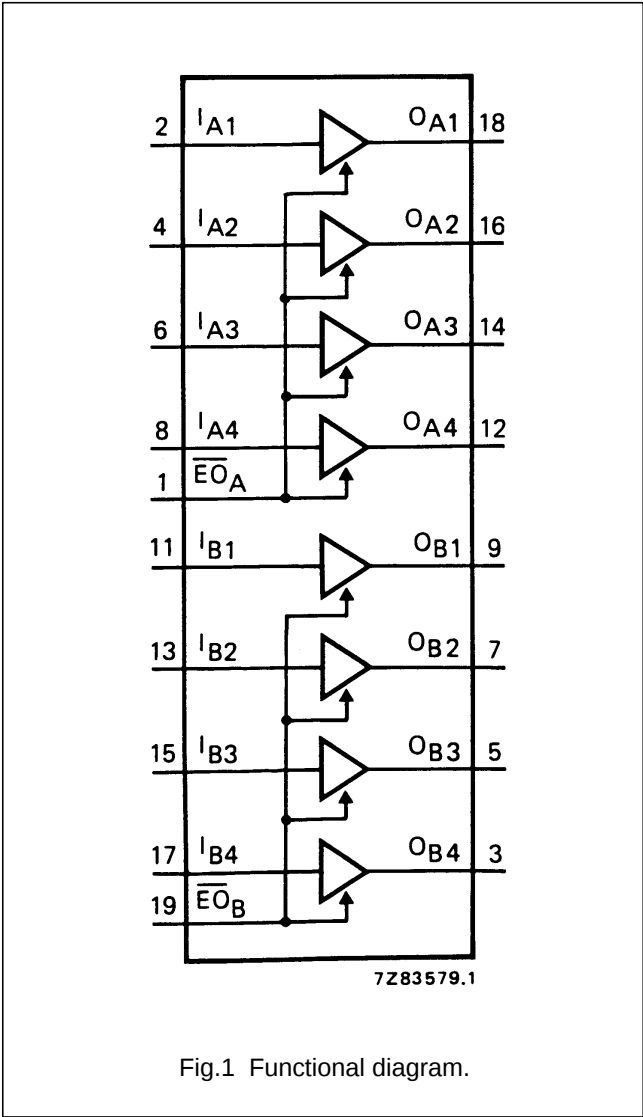
HEF40244B
buffers

DESCRIPTION

The HEF40244B is an octal non-inverting buffer with 3-state outputs. It features output stages with high current output capability suitable for driving highly capacitive loads.

The 3-state outputs are controlled by the output enable inputs $\overline{EO}_A$ and $\overline{EO}_B$. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state. The device also features hysteresis on all inputs to improve noise immunity. Schmitt-trigger action in the inputs makes the circuit highly tolerant to slower input rise and fall times.

The HEF40244B is pin and functionally compatible with the TTL '244' device.



HEF40244BP(N): 20-lead DIL; plastic (SOT146-1)
HEF40244BD(F): 20-lead DIL; ceramic (cerdip) (SOT152)
HEF40244BT(D): 20-lead SO; plastic (SOT163-1)
(): Package Designator North America

PINNING

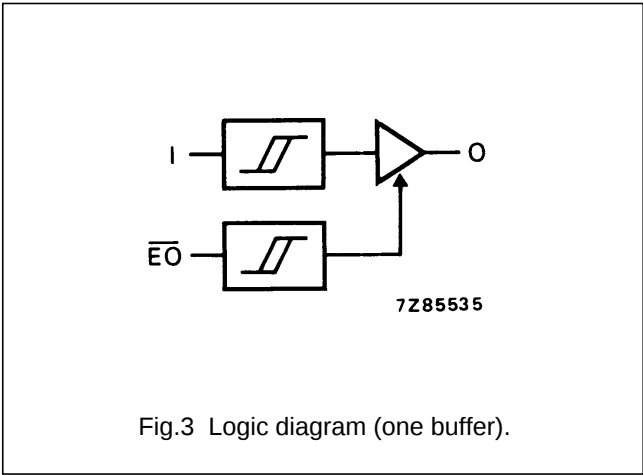
I_{A1} to I_{A4}	inputs
I_{B1} to I_{B4}	inputs
O_{A1} to O_{A4}	bus outputs
O_{B1} to O_{B4}	bus outputs
$\overline{EO}_A$, $\overline{EO}_B$	output enable inputs (active LOW)

FAMILY DATA, I_{DD} LIMITS category buffers

See Family Specifications

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TRUTH TABLE

INPUTS		OUTPUT
I _n	$\overline{EO}$	O _n
H	L	H
L	L	L
X	H	Z

Notes

- 1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance off state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
See Family Specifications, except for:

D.C. current into any input	$\pm I_i$	max.	10 mA
D.C. source or sink current into any output	$\pm I_o$	max.	25 mA
D.C. current into the supply terminals	$\pm I$	max.	100 mA

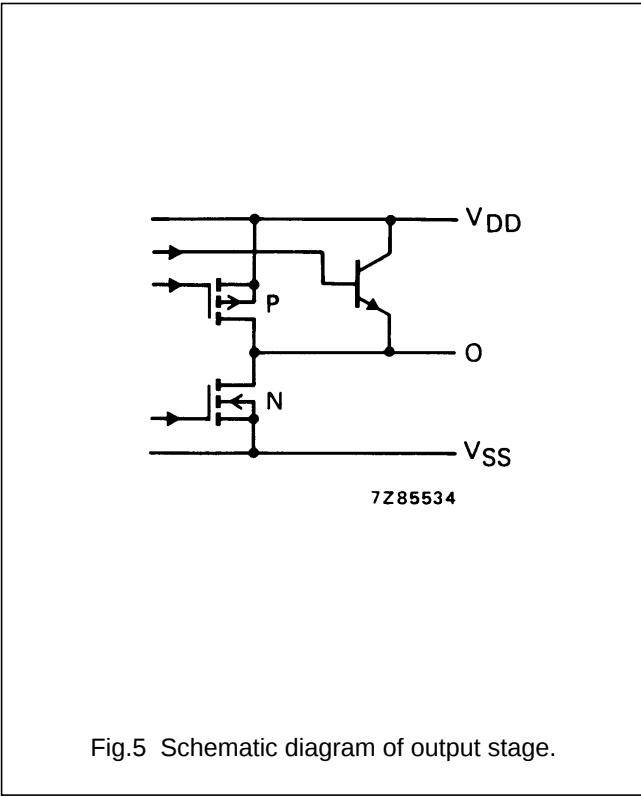
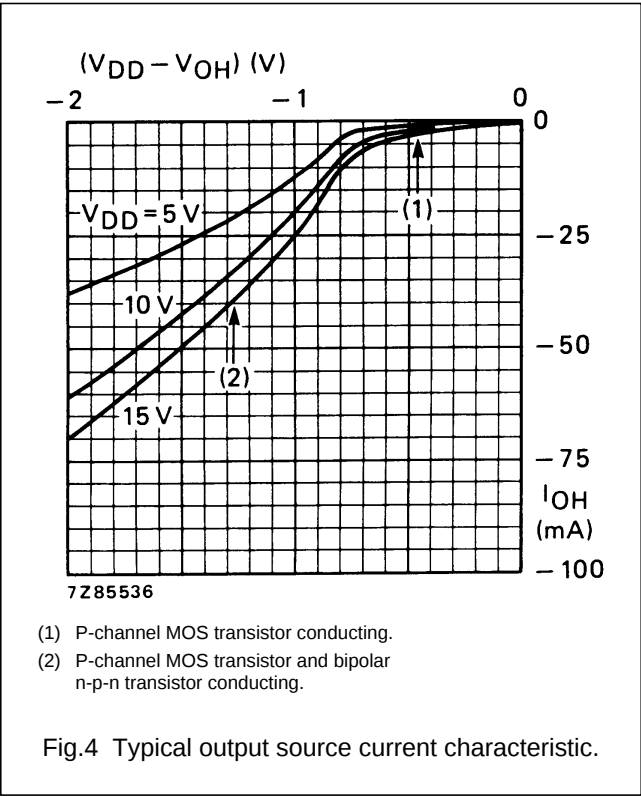
DC CHARACTERISTICS

V_{SS} = 0 V

	V _{DD} V	V _{OH} V	V _{OL} V	SYMBOL	T _{amb} (°C)					
					-40		+25		+85	
					MIN.	TYP.	MIN.	TYP.	MIN.	TYP.
Output current HIGH	5	4,6		-I _{OH}	0,75		0,6	1,2	0,45	mA
	10	9,5			1,85		1,5	3,0	1,1	mA
	15	13,5			14,5		15	50	15,5	mA
Output current HIGH	5	3,6		-I _{OH}	9,3		10	24	10,7	mA
	10	8,4			14,4		15	46	15,0	mA
	15	13,2			19,5		20	62	19,8	mA
Output current LOW	5		0,4	I _{OL}	2,9		2,3	5,4	1,75	mA
	10		0,5		9,5		7,6	17	5,50	mA
	15		1,5		30,0		25	45	19,0	mA
Hysteresis voltage (any input)	5			V _H			220			mV
	10						250			mV
	15						320			mV

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AC CHARACTERISTICS

VSS = 0 V; Tamb = 25 °C; input transition times ≤ 20 ns

ALL BUFFERS SWITCHING	VDD V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$4\,250 f_i + \sum (f_o C_L) \times V_{DD}^2$	where fi = input freq. (MHz) fo = output freq. (MHz) CL = load capacitance (pF) Σ (foCL) = sum of outputs VDD = supply voltage (V)
	10	$17\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$46\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_{An/Bn} \rightarrow O_{An/Bn}$ HIGH to LOW	5	t_{PHL}		95	190 ns	83 ns + (0,24 ns/pF) C_L
	10			40	80 ns	35 ns + (0,10 ns/pF) C_L
	15			30	60 ns	26 ns + (0,07 ns/pF) C_L
	5	t_{PLH}		85	170 ns	82 ns + (0,06 ns/pF) C_L
	10			40	80 ns	38 ns + (0,03 ns/pF) C_L
	15			30	60 ns	29 ns + (0,02 ns/pF) C_L
Output transition times HIGH to LOW	5	t_{THL}		40	80 ns	see Fig.6
	10			20	40 ns	
	15			15	30 ns	
	5	t_{TLH}		30	60 ns	
	10			20	40 ns	
	15			15	30 ns	
3-state propagation delays Output disable times $\overline{EO} \rightarrow O_{An/Bn}$ HIGH	5	t_{PHZ}		70	140 ns	
	10			35	70 ns	
	15			30	60 ns	
	5	t_{PLZ}		75	150 ns	
	10			40	80 ns	
	15			30	60 ns	
Output enable times $\overline{EO} \rightarrow O_{An/Bn}$ HIGH	5	t_{PZH}		80	160 ns	
	10			35	70 ns	
	15			30	60 ns	
	5	t_{PZL}		90	180 ns	
	10			40	80 ns	
	15			30	60 ns	

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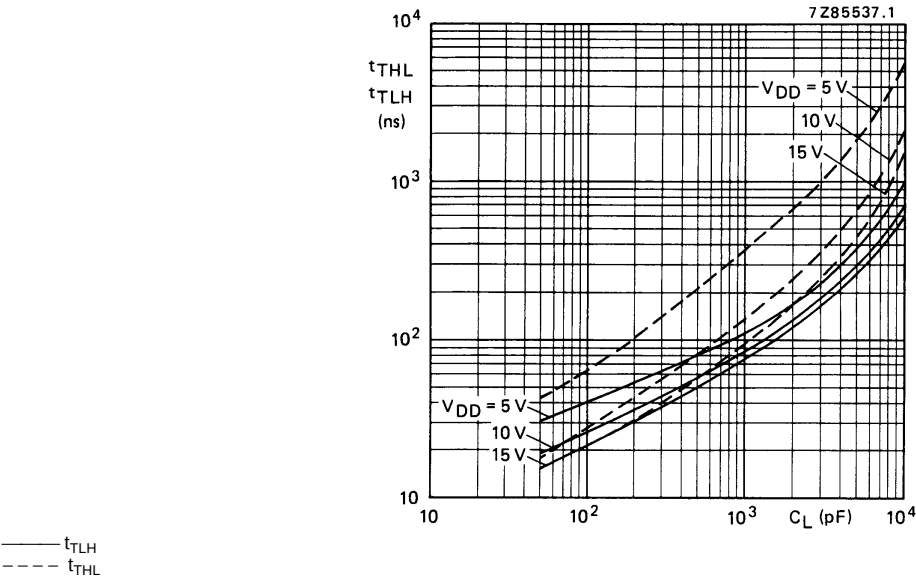


Fig.6 Output transition times as a function of the load capacitance.